REMARKS

Claims 2, 4-12, 14 and 28-31 are pending in this application, of which claims 2, 4, 7-9 and 28-31 have been withdrawn from consideration. Claim 13 has been herein canceled. Claims 5, 10 and 11 have been herein amended. Reconsideration of the rejections in view of these amendments and the following remarks is respectfully requested.

Claim Objections

Claims 10 and 11 were objected to because of informalities.

In the claims and the specification, the term "scrapping" has been replaced with "strapping".

Claim Rejections – 35 U.S.C. §112

Claims 10-13 were rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement.

Claim 13 has been canceled and the rejection of the claim has become moot. Also, Applicant respectfully traverses this rejection with respect to claims 10-12.

The Examiner alleged that there is no support in the embodiment of FIGs. 30-31 for a strapping word line, a shield electrode and a second wiring, as recited in claims 10-13, respectively.

However, as described in page 53, line 18 to page 56, line 13 of the specification, the sixth embodiment is for improving the alignment allowance of the bit line contact hole in the semiconductor memory device according to the first, second and fifth embodiments of the present

application (see page 53, lines 18-20). The sixth embodiment shows just an example applied to the first embodiment and is not intended to limit to the application to the particular embodiment. These disclosures clearly show to a person of ordinary skill in the art that the sixth embodiment is applicable to the first, the second and the fifth embodiments.

The strapping word line is described in the first embodiment (see FIGs. 1, 7 and 8), in the second embodiment (see FIG. 9) and in the fifth embodiment (see FIG. 24). The shield electrode is described in the first embodiment (see FIG. 7).

Thus, there is a support in the embodiment of FIGs. 30-31 for the strapping word line (claims 10 and 11) and the shield electrode (claim 12).

For at least these reasons, the 35 U.S.C. §112, first paragraph, rejection of claims 10-12 should be withdrawn.

Claim Rejection – 35 U.S.C. §102

Claims 5, 6, 10, 11, 13 and 14 were rejected under 35 U.S.C. § 102(e) as being anticipated by Hamamoto et al (U.S. Patent No. 5,895,946).

Applicant respectfully traverses this rejection.

In order to further clarify the present invention, claim 5 has been amend to recite, among other things, "a **semiconductor layer** having a first diffused region and a second diffused region formed therein and having substantially **flat surfaces**, said semiconductor layer defining a first side and a second side; a transistor having **a gate electrode formed only on said first side** of the semiconductor layer between the first and the second diffused regions with an insulation film interposed therebetween; and **a capacitor formed only on said first side** of the semiconductor

layer and having a storage electrode connected to the first diffused region; **a bit line formed on said second side** of the semiconductor layer, and extended in a direction normal to the gate electrode; and **a support substrate formed on said first side** of the semiconductor layer for supporting the device layer; the semiconductor layer including a first region which is extended in the extending direction of the bit line and includes the first diffused region and the second diffused region, and a second region which is adjacent to the first region on a side of an extending direction of the gate electrode and includes the second diffused region."

The Examiner alleged that Hamamoto et al teaches in FIG. 88A a memory device comprising: a device layer including a silicon layer 211, 212 having first and second diffusion regions formed therein, a gate electrode 207 formed through an insulating film 206 on one side of the silicon layer between the first and second diffusion regions, a capacitor 215 formed on the one side of the silicon layer and having a storage electrode 205 connected to the first diffusion region.

However, in the semiconductor memory device of Hamamoto et al, the silicon layer 211, 212 does not have substantially flat surfaces. The capacitor is formed on the second side of the silicon layer 211, 212 opposed to the first side that the gate electrode 207 is formed. The bit line 208 and the gate electrode 207 are formed on same first side of the silicon layer 211, 212. The support substrate 219 is formed on the second side of the silicon layer 211, 212. These features of Hamamoto et al are clearly different from the present invention.

In the present invention, the semiconductor layer has substantially flat surfaces. The capacitor is formed on the first side of the semiconductor layer. The bit line is formed on the second side of the semiconductor layer. The support substrate is formed on the first side of the semiconductor layer.

Thus, the Hamamoto et al does not teach or suggest, among other things, "a **semiconductor layer** having a first diffused region and a second diffused region formed therein and having substantially **flat surfaces**, said semiconductor layer defining a first side and a second side; a transistor having a **gate electrode formed only on said first side** of the semiconductor layer between the first and the second diffused regions with an insulation film interposed therebetween; and **a capacitor formed only on said first side** of the semiconductor layer and having a storage electrode connected to the first diffused region; **a bit line formed on said second side** of the semiconductor layer, and extended in a direction normal to the gate electrode; and **a support substrate formed on said first side** of the semiconductor layer for supporting the device layer" as recited in amended claim 5.

For at least these reasons, claim 5 patentably distinguishes over Hamamoto et al. Claims 6, 10, 11 and 14, depending from claim 5, also patentably distinguish over Hamamoto et al for at least the same reasons.

Thus, the 35 USC §102(b) rejection should be withdrawn.

Claim Rejection – 35 U.S.C. §103

Claim 12 was rejected under 35 U.S.C. §103(a) as being unpatentable over Hamamoto et al in view of Ajika et al (U.S. Patent No. 5,798,289).

Applicant respectfully traverses this rejection.

As described above, claim 5 patentably distinguishes over Hamamoto et al. Ajika et al has been cited for allegedly disclosing "a shield electrode formed above the bit line for suppressing

interference between the bit lines. Such disclosure, however, does not remedy the deficiencies of Hamamoto et al.

For at least these reasons, claim 12 patentably distinguishes over Hamamoto et al and Ajika et al.

Thus, the 35 USC §103(a) rejection should be withdrawn.

Withdrawn Claims 7-9

Although claims 7-9 have been withdrawn from consideration, these claims depend from, directly or indirectly, claim 5. Because claim 5 is patentable as discussed above, claims 7-9 also are patentable for at least the same reasons.

It is submitted that nothing in the cited references, taken either alone or in combination, teaches or suggests all the features recited in each claim of the present invention. Thus all pending claims are in condition for allowance. Reconsideration of the rejections, withdrawal of the rejections and an early issue of a Notice of Allowance are earnestly solicited.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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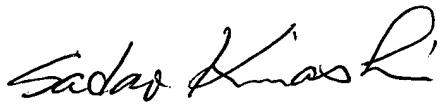

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